REMARKS

I. Status Summary

Claims 1 and 3 are pending in the present application. Claims 1 and 3 have been amended. Therefore, upon entry of this amendment, Claims 1 and 3 will be pending. No new matter has been introduced by the present amendment. Reconsideration of the application as amended and based on the arguments set forth hereinbelow is respectfully requested.

Support for the claim amendments can be found throughout the present application. For example, support for the claim amendments can be found at page 15, lines 12-37.

II. Claim Interpretation

The Examiner states that Claim 3 is an apparatus claim that contains multiple instances of functional language. Further, the Examiner states that these features do not structurally distinguish claim subject matter from prior art, and thus do not define patentable differences. In particular, the Examiner points to the Claim 3 features of "an instruction decoder for decoding a processor instruction that contains an instruction opcode" (emphasis added) and "a post condition, which specifies that a conditional jump is to be processed and the corresponding flag bits of an arithmetic-logic unit are to be checked" (emphasis added). (See page 2, of the Official Action).

Element (a) of Claim 3 has been amended to replace the phrase "an instruction decoder for decoding a processor instruction that contains an instruction opcode" with the phrase "an instruction decoder operable to decode a processor instruction that

contains an instruction opcode". Applicant respectfully submits that the new language of "operable to decode" in place of "for decoding" adds structural language to the phrase that adds structural distinction over prior art.

Further, element (a) of Claim 3 has been amended to replace "a post condition, which specifies that a conditional jump is to be processed and the corresponding flag bits of an arithmetic-logic unit are to be checked" with "a post-condition configured specifying a conditional jump is processed and the corresponding flag bits of an arithmetic-logic unit are to be checked". Applicant respectfully submits that the new language of "post-condition configured to specify" in place of "post-condition, which specifies that" adds structural distinction over prior art.

Accordingly, applicant respectfully submits that Claim 3 properly recites structural language.

III. Claim Rejections Under 35 U.S.C. § 103

Claims 1 and 3 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over EPO No. 0130381 to Auslander (hereinafter, "Auslander"), in view of U.S. Patent No. 4,907,192 to Keneko (hereinafter, "Keneko"), and further in view of Mahlke et al., "A Comparison of Full and Partial Predicated Execution Support for ILP Processors" (hereinafter, "Mahlke"). This rejection is respectfully traversed in view of the above amendments and the below remarks.

Claim 1 recites a method for processing conditional jump instructions in a processor with pipeline computer architecture. Further, claim 1 has been amended to recite loading and decoding a processor instruction that contains an instruction

opcode, register addresses, a relative jump distance, a precondition, which specifies under which conditions the instruction is actually to be executed, and a post-condition, which specifies that a conditional jump is to be processed and the corresponding flag bits of an arithmetic-logic unit are to be checked. Further, Claim 1 recites that the post-condition comprises a plurality of post-condition bits that are checked in the processor. Claim 1 has been amended to recite checking the precondition, and execution of the decoded processor instruction if the precondition is fulfilled. Further, Claim 1 has been amended to recite that, in the case of a fulfilled precondition, checking the post-condition, and carrying out no-jump of the post-condition if not fulfilled, and checking the corresponding flag bits, if the post-condition is fulfilled. Further, Claim 1 recites jumping to a jump address as a function of the relative jump distance contained in the processor instruction if the post-condition is fulfilled and the checked flag bits are set. Summarily, neither Auslander, Keneko nor Mahlke, alone or in combination, teaches or suggests each and every feature as recited by amended Claim 1.

Auslander is directed to a mechanism for fully executing a branch-on-any-bit-in-any-register instruction within one machine cycle of a host computing system. Means are provided whereby a branch decision may be made not only on a specified bit in the condition register, but on any bit in any of the general purpose registers provided in the system central processing unit (CPU). Means are also provided for saving a given configuration of the condition register in the general purpose registers for later use in subsequent branch-on-bit operations.

In the sections of Auslander cited by the Examiner, the use of a branch instruction (BI) field is described. In particular and with reference to page 33, lines 7-33 of Auslander:

> "A bit, whose position is specified by the BI field, is selected from register RA if RA is not 0, or from CR if RA is 0. If the bit is a 1, then the address of the next instruction is computed by the sum of the address of this instruction and the sign-extended D field. If it is a 0 the execution continues sequentially."

The BI field functions as a pointer to one bit of a certain register, RA or CR (the first step). Then, it is checked if the bit of RA or CR to which the BI field points is 1 or 0 (the second step). If the bit is 1, the next instruction is computed by the sum of the address of this instruction and the sign-extended D field. Alternatively, if the bit is 0, the execution continues sequentially (the third step). As such, three steps are needed in Auslander to determine which instruction should follow after the actual decoded instruction.

In contrast to the claimed subject matter, Auslander neither teaches nor suggests the Claim 1, element (a) feature of a post-condition being part of a processor instruction and the Claim 1 element (c) feature of, in the case of a fulfilled precondition, checking the post-condition, and carrying out no-jump of the post-condition if not fulfilled. These features of the claimed subject matter are advantageous, for example, because the processor is able to quickly check whether the post-condition is fulfilled. In contrast to these features, Auslander teaches a pointer BI to the bit which determines whether a jump has to be implemented. In contrast, the claimed subject matter requires only a single step to determine that execution continues sequentially.

As set forth above, Auslander requires three steps. Thus, the claimed subject matter has an advantage of speed over Auslander. Accordingly, it is respectfully submitted that Auslander does not teach or suggest the claimed features of a post-condition being part of a processor instruction, and, in the case of a fulfilled precondition, checking the post-condition, and carrying out no-jump of the post-condition if not fulfilled.

Further, Auslander fails to teach or suggest a post-condition as recited by Claim 1. In particular, Auslander teaches that the BI field is a pointer, not a condition which specifies a conditional jump itself, as required by Claim 1. Accordingly, the BI field taught by Auslander cannot correspond to the post-condition as required by Claim 1.

Auslander also fails to teach or suggest the Claim 1, element (c) feature of checking flag bits corresponding to a post-condition if the post-condition is fulfilled. As such, Auslander fails to teach or suggest the features required by element (c) of Claim 1.

Keneko fails to overcome the significant shortcomings of Auslander to teach or suggest the claimed subject matter. The Examiner stated that Keneko teaches adding a condition selector to receive flag bits, and, based on an instruction specified in condition bits, to perform appropriate checks of the flags. (See page 5, of the Official Action). However, Keneko fails to teach or suggest the Claim 1, element (a) feature of a post-condition being part of a processor instruction and the Claim 1 element (c) feature of, in the case of a fulfilled precondition, checking the post-condition, and carrying out no-jump of the post-condition if not fulfilled. Further, Keneko fails to teach

or suggest the Claim 1, element (c) feature of checking flag bits corresponding to a post-condition if the post-condition is fulfilled.

Mahlke fails to overcome the significant shortcomings of Auslander and Keneko to teach or suggest the claimed subject matter. The Examiner stated that Mahlke teaches an instruction containing a precondition, which specifies under which conditions the instruction is actually to be executed, and the step of the execution of the decoded processor instruction if the precondition is fulfilled. (See page 6, of the Official Action). However, Mahlke fails to teach or suggest the Claim 1, element (a) feature of a post-condition being part of a processor instruction and the Claim 1 element (c) feature of, in the case of a fulfilled precondition, checking the post-condition, and carrying out no-jump of the post-condition if not fulfilled. Further, Mahlke fails to teach or suggest the Claim 1, element (c) feature of checking flag bits corresponding to a post-condition if the post-condition is fulfilled.

For the reasons set forth above, applicant respectfully submits that neither Auslander, Keneko, nor Mahlke, alone or in combination, teach or suggest each and every feature required by Claim 1. For this reason, applicant respectfully submits that Claim 1 is not obvious in view of Auslander, Keneko, and Mahlke. Therefore, applicant respectfully requests that the rejection of Claim 1 under 35 U.S.C. § 103(a) be withdrawn and the claim allowed at this time.

Claim 3 recites an apparatus for processing conditional jump instructions in a processor with pipeline computer architecture. Further, Claim 3 has been amended to recite an instruction decoder operable to decode a processor instruction that contains an instruction opcode, register addresses, a relative jump distance, a precondition

configured to specify conditions the instruction is actually executed, and a post-condition configured to specify a conditional jump is processed and the corresponding flag bits of an arithmetic-logic unit are to be checked. Claim 3 also recites that the post-condition comprises a plurality of post-condition bits that are checked in the processor. Further, Claim 3 recites that the instruction decoder is operable to check, in the case of a fulfilled precondition, whether the post-condition is fulfilled. Claim 3 has been amended to recite that, if the post-condition is fulfilled, checking corresponding flag bits, and if positive, driving a program counter for forming a jump address as a function of the relative jump distance contained in the processor instruction. Summarily, neither Auslander, Keneko nor Mahlke, alone or in combination, teaches or suggests each and every feature as recited by amended Claim 3.

Similar to Claim 1, Claim 3 recites an instruction decoder operable to decode a processor instruction that contains an instruction opcode, register addresses, a relative jump distance, a precondition, and a post-condition. Further, similar to Claim 1, Claim 3 recites that the precondition is configured to specify under which conditions the instruction is actually executed. In addition, similar to Claim 1, Claim 3 recites that the post-condition is configured to specify that a conditional jump is processed and the corresponding flag bits of an arithmetic logic unit are to be checked. Further, similar to Claim 1, Claim 3 recites that the post-condition comprises a plurality of post-condition bits that are checked in the processor. Claim 3 has also been amended similar to Claim 1 to recite that, if the post-condition is fulfilled, corresponding flag bits are checked. For the reasons provided above, Auslander, Keneko, and Mahlke fail to

teach or suggest these features. Therefore, applicant respectfully submits that Claim 3 is not obvious in view of Auslander, Keneko, and Mahlke. Therefore, applicant respectfully requests that the rejection of Claim 3 under 35 U.S.C. § 103(a) be withdrawn and the claim allowed at this time.

Summarily, the presently claimed subject matter comprises at least two main advantages compared to the cited references. First, a very fast detection for a sequential execution is provided if the post-condition is not fulfilled. Second, additional complex condition settings are feasible by means of the plurality of checked flag bits of the arithmetic-logic unit.

CONCLUSION

In light of the above amendments and remarks, it is respectfully submitted that the present application is now in proper condition for allowance, and an early notice to such effect is earnestly solicited.

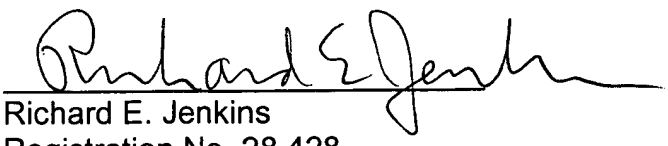
If any small matter should remain outstanding after the Patent Examiner has had an opportunity to review the above amendments and remarks, the Patent Examiner is respectfully requested to telephone the undersigned patent attorney in order to resolve these matters and avoid the issuance of another Official Action.

DEPOSIT ACCOUNT

The Commissioner is hereby authorized to charge any fees associated with the filing of this correspondence to Deposit Account No. **50-0426**.

Respectfully submitted,

JENKINS, WILSON, TAYLOR & HUNT, P.A.

Date: September 20, 2006 By: 

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